IEC 61691-6

Edition 2.0 2021-06

INTERNATIONAL STANDARD

IEEE Std 1076.1™

Behavioural languages – Part 6: VHDL Analog and Mixed-Signal Extensions

INTERNATIONAL ELECTROTECHNICAL COMMISSION

ICS 25.040.01; 35.060

ISBN 978-2-8322-9830-5

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BEHAVIOURAL LANGUAGES –

Part 6: VHDL Analog and Mixed-Signal Extensions

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IEEE Std	FDIS	Report on voting
1076.1 (2017)	91/1715/FDIS	91/1727/RVD

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IEEE Std 1076.1™-2017
(Revision of
IEEE Std 1076.1-2007)

IEEE Standard VHDL Analog and Mixed-Signal Extensions

Sponsor

Design Automation Standards Committee
of the
IEEE Computer Society

Approved 28 September 2017

IEEE-SA Standards Board

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Abstract: The IEEE 1076.1 language, a hardware description language for the description and the simulation of analog, digital, and mixed-signal systems, is defined in this standard. The language, also informally known as VHDL-AMS, is built on IEEE Std 1076-2008 (VHDL) and extends it with additions and changes to provide capabilities of writing and simulating analog and mixed-signal models.

Keywords: analog design, computer, computer languages, hardware design, IEEE 1076™, IEEE 1076.1™, mixed-signal design, VHDL

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Introduction

This introduction is not part of IEEE Std 1076.1-2017, IEEE Standard VHDL Analog and Mixed-Signal Extensions.

The IEEE 1076.1 language, informally known as VHDL-AMS, is a superset of IEEE Std 1076-2008 (VHDL) that provides capabilities for describing and simulating analog and mixed-signal systems with conservative and nonconservative semantics for the analog portion of the system.[1] The language supports modeling at many abstraction levels in electrical and nonelectrical energy domains for lumped systems that can be described by ordinary differential equations and algebraic equations. The language does not specify any particular technique to solve the equations, but it rather defines the results that must be achieved. The solution of the equations may include discontinuities. Interaction between the digital part of a model and its analog part is supported in a flexible and efficient manner. Finally, support for frequency domain small-signal and noise simulation is provided.

The extension of VHDL to support analog and mixed-signal systems began in 1989, as part of the second revision of IEEE Std 1076 targeted for a 1993 release. A large number of requirements to support analog and mixed-signal systems were submitted, and it soon became apparent that the complexity of the topic required the formation of a separate working group. The design of the IEEE 1076.1 language formally began in 1993, when the IEEE 1076.1 Working Group was formed under the auspices of the Design Automation Standards Committee of the IEEE Computer Society, under Project Authorization Request (PAR) 1076.1. Its charter was to extend the IEEE 1076 (VHDL) language to support the requirements for the description and simulation of analog and mixed-signal systems. The IEEE 1076.1 Working Group approved the draft standard in June 1997. The first release of the draft of IEEE Std 1076.1-1999 was approved by the IEEE Standards Board on 18 March 1999.

The 2017 revision includes changes made to IEEE Std 1076 since the publication of IEEE Std 1076.1-2007, as well as additions to the language. See the Annex E for a list of changes from the 2007 release.

The IEEE 1076.1 Working Group will continue to maintain the IEEE 1076.1 language.[2]

[1] Information on references can be found in Clause 2.

[2] Information on these efforts may be found at the following URL: http://www.eda-twiki.org/vhdl-ams.

IEEE Standard VHDL Analog and Mixed-Signal Extensions

1. Overview

1.1 Scope

This standard defines the IEEE 1076.1™ language, a hardware description language for the description and the simulation of analog, digital, and mixed-signal systems. Informally called VHDL-AMS (VHSIC Hardware Description Language for Analog and Mixed-Signal, where VHSIC stands for Very High Speed Integrated Circuits), the language is built on the IEEE 1076™ (VHDL) language and extends it to provide capabilities of writing and simulating analog and mixed-signal models.

1.2 Purpose

To support the design and verification of complex electronic systems containing a mixture of analog and digital devices, the IEEE 1076.1 language provides, as an extension of the IEEE VHDL 1076 language, a comprehensive set of capabilities for the description and simulation of mixed-signal and mixed-technology systems.

The revision adds selected new features to the language definition of IEEE Std 1076.1-2007, and it updates that standard to reflect changes in the VHDL specification, IEEE Std 1076-2008.[1]

1.3 Structure and terminology of this standard

1.3.1 General

This document contains the complete reference of the IEEE 1076.1 VHDL language, including the unchanged portions of the base language and the extensions. Formally, IEEE Std 1076.1-2017 defines the extensions only, consisting of additions to, and changes of, the text of IEEE Std 1076-2008. The corresponding text is highlighted in light gray. Text that is not highlighted is identical in this document and in IEEE Std 1076-2008.

This standard is organized into clauses, each of which focuses on some particular area of the language. Within each clause, individual constructs or concepts are discussed in each subclause.

[1]Information on references can be found in Clause 2.

Each subclause describing a specific construct begins with an introductory paragraph. Next, the syntax of the construct is described using one or more grammatical *productions*.

A set of paragraphs describing the meaning and restrictions of the construct in narrative form then follow.

In this document, the word *shall* is used to indicate a mandatory requirement. The word *should* is used to indicate a recommendation. The word *may* is used to indicate a permissible action. The word *can* is used for statements of possibility and capability.

Finally, each clause may end with examples, notes, and references to other pertinent clauses.

1.3.2 Syntactic description

The form of a VHDL description is described by means of context-free syntax using a simple variant of the Backus-Naur form (BNF); in particular:

a) Lowercase words in roman font, some containing embedded underlines, are used to denote syntactic categories, for example:

    formal_port_list

   Whenever the name of a syntactic category is used, apart from the syntax rules themselves, spaces take the place of underlines [thus, “formal port list” would appear in the narrative description when referring to the syntactic category in item a)].

b) Boldface words are used to denote reserved words, for example:

    array

   Reserved words shall be used only in those places indicated by the syntax.

c) A *production* consists of a *left-hand side*, the symbol “::=” (which is read as “can be replaced by”), and a *right-hand side*. The left-hand side of a production is always a syntactic category; the right-hand side is a replacement rule. The meaning of a production is a textual-replacement rule: any occurrence of the left-hand side may be replaced by an instance of the right-hand side.

d) A vertical bar (|) separates alternative items on the right-hand side of a production unless it occurs immediately after an opening brace, in which case it stands for itself, as follows:

    letter_or_digit ::= letter | digit
    choices ::= choice { | choice }

   In the first instance, an occurrence of “letter_or_digit” can be replaced by either “letter” or “digit.” In the second case, “choices” can be replaced by a list of “choice,” separated by vertical bars [see item f) for the meaning of braces].

e) Square brackets [ ] enclose optional items on the right-hand side of a production; thus, the following two productions are equivalent:

    return_statement ::= **return** [expression] ;
    return_statement ::= **return** ; | **return** expression ;

   Note, however, that the initial and terminal square brackets in the right-hand side of the production for signatures (see 4.5.3) are part of the syntax of signatures and do not indicate that the entire right-hand side is optional.

f) Braces { } enclose a repeated item or items on the right-hand side of a production. The items may appear zero or more times; the repetitions occur from left to right as with an equivalent left-recursive rule. Thus, the following two productions are equivalent:

    term ::= factor { multiplying_operator factor }
    term ::= factor | term multiplying_operator factor

g) If the name of any syntactic category starts with an italicized part, it is equivalent to the category name without the italicized part. The italicized part is intended to convey some semantic

information. For example, *type*_name and *subtype*_name are both syntactically equivalent to name alone.

h) The term simple_name is used for any occurrence of an identifier that already denotes some declared entity.

1.3.3 Semantic description

The meaning and restrictions of a particular construct are described with a set of narrative rules immediately following the syntactic productions. In these rules, an italicized term indicates the definition of that term, and identifiers appearing entirely in uppercase letters refer to definitions in package STANDARD (see 16.3).

The following terms are used in these semantic descriptions with the following meanings:

erroneous: The condition described represents an ill-formed description; however, implementations are not required to detect and report this condition. Conditions are deemed erroneous only when it is impossible in general to detect the condition during the processing of the language.

error: The condition described represents an ill-formed description; implementations are required to detect the condition and report an error to the user of the tool.

illegal: A synonym for “error.”

legal: The condition described represents a well-formed description.

1.3.4 Front matter, examples, notes, references, and annexes

Prior to this subclause are several pieces of introductory material; following Clause 24 are some annexes and an index. The front matter, annexes (except Annex B), and index serve to orient and otherwise aid the user of this standard, but are not part of the definition of VHDL; Annex B, however, is normative.

Some clauses of this standard contain examples, notes, and cross-references to other clauses of the standard; these parts always appear at the end of a clause. Examples are meant to illustrate the possible forms of the construct described. Illegal examples are italicized. Notes are meant to emphasize consequences of the rules described in the clause or elsewhere. In order to distinguish notes from the other narrative portions of this standard, notes are set as enumerated paragraphs in a font smaller than the rest of the text. Cross-references are meant to guide the user to other relevant clauses of the standard. Examples, notes, and cross-references are not part of the definition of the language.

1.3.5 Incorporation of Property Specification Language

VHDL incorporates the simple subset of the Property Specification Language (PSL) as an embedded language for formal specification of the behavior of a VHDL description. PSL is defined by IEEE Std 1850™-2005. All PSL constructs that appear in a VHDL description shall conform to the VHDL flavor of PSL. Within this standard, reference is made to syntactic rules of PSL. Each such reference has the italicized prefix *PSL_* and corresponds to the syntax rule in IEEE Std 1850-2005 with the same name but without the prefix.

2. Normative references

The following referenced documents are indispensable for the application of this document (i.e., they must be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

IEEE Std 754™-1985 (Reaff 1990), IEEE Standard for Binary Floating-Point Arithmetic.[2, 3]

IEEE Std 854™-1987 (Reaff 1994), IEEE Standard for Radix-Independent Floating-Point Arithmetic.

IEEE Std 1076™-2008, IEEE Standard VHDL Language Reference Manual.

IEEE Std 1850™-2005, IEEE Standard for Property Specification Language (PSL).

IEEE/ASTM SI 10™, American National Standard for Metric Practice.[4]

ISO/IEC 8859-1:1998, Information technology—8-bit single-byte coded graphic character sets—Part 1: Latin alphabet No. 1.[5]

ISO/IEC 9899:1999, Programming Languages—C.

ISO/IEC 9899:1999/Cor 1:2001, Programming languages—C, Technical Corrigendum 1.

ISO/IEC 9899:1999/Cor 2:2004, Programming languages—C, Technical Corrigendum 2.

ISO/IEC 19501:2005, Information technology—Open Distributed Processing—Unified Modeling Language (UML) Version 1.4.2.

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